(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 February 2004 (12.02.2004)

PCT

(10) International Publication Number
WO 2004/013682 A3

(51) International Patent Classification[7]: G09G 3/36, G02F 0/00, 1/133

(21) International Application Number: PCT/KR2003/001549

(22) International Filing Date: 31 July 2003 (31.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10-2002-0045815 2 August 2002 (02.08.2002) KR

(71) Applicant *(for all designated States except US)*: SAMSUNG ELECTRONICS CO., LTD. [KR/KR]; 416, Maetan-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do 442-742 (KR).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: KIM, Jong-Seon [KR/KR]; Dongbu Apt. 102-301, Dokgok-dong, Pyeongtaek-city, Kyungki-do 459-801 (KR).

(74) Agent: YOU ME PATENT & LAW FIRM; Teheran Bldg., 825-33, Yoksam-dong, Kangnam-ku, Seoul 135-080 (KR).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

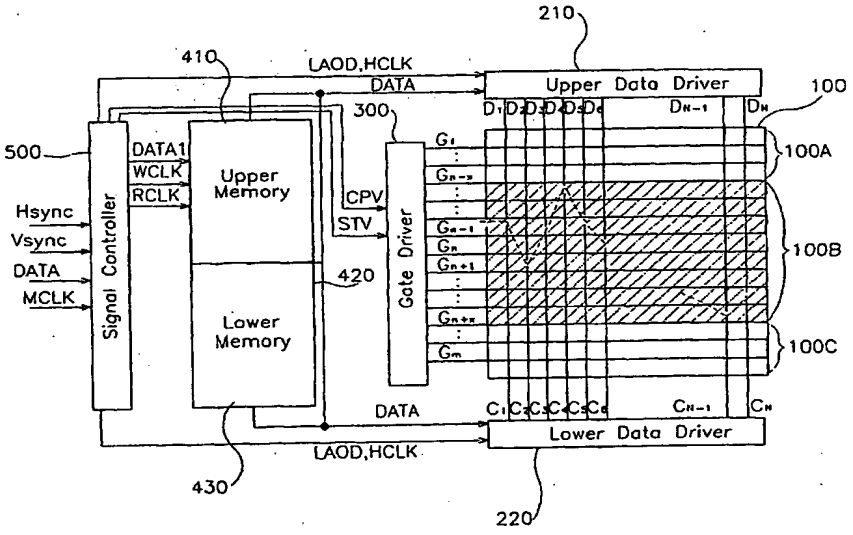
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*

(88) Date of publication of the international search report:
2 December 2004

*[Continued on next page]*

(54) Title: LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF




(57) Abstract: An LCD includes a plurality of upper (G1-Gn-x-1), middle (Gn-x-Gn+x), and lower (Gn+x+1-Gm) gate lines transmitting scanning signals provided on upper (100A), middle (100B), and lower (100C) areas, respectively, a plurality of pairs of upper (D1-Dn) and lower (C1-Cn) data lines transmitting data voltages, and a plurality of pixels connected to the gate lines (G1-Gm) and the data lines (D1-Dn and (C1-Cn). The pixels are arranged in a matrix and include upper, middle, and lower pixels provided on the upper, the middle, and the lower areas, respectively. Each pair of upper and lower data lines are separated from each other at a disconnection, and the disconnections of the upper and the lower data lines are randomly distributed on the middle area.

WO 2004/013682 A3

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# INTERNATIONAL SEARCH REPORT

International Application No.
PCT/[redacted]03/001549

CLASSIFICATION OF SUBJECT MATTER

IPC[7]: G09G 3/36, G02F 0/00, G02F 1/133

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[7]: G09G, G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC, PAJ, WPI, English Fulltext

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 2002/0084965 A1 (PARK) 4 July 2002 (04.07.2002) *the whole document, esp. fig. 3.* | 1 - 15 |
| A | US 2002/0063671 A1 (KNAPP) 30 May 2002 (30.05.2002) *the whole document, esp. abstact; fig. 2.* | 1 - 15 |
| A | JP 2001 343922 A (SHARP KK) 14 December 2001 (14.12.2001) *abstract, fig. 1.* | 1 - 15 |

---

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

„A" document defining the general state of the art which is not considered to be of particular relevance

„E" earlier application or patent but published on or after the international filing date

„L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

„O" document referring to an oral disclosure, use, exhibition or other means

„P" document published prior to the international filing date but later than the priority date claimed

„T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

„X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

„Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

„&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 18 August 2004 (18.08.2004) | 3 September 2004 (03.09.2004) |
| Name and mailing adress of the ISA/AT<br>Austrian Patent Office<br>Dresdner Straße 87, A-1200 Vienna<br>Facsimile No. 1/53424/535 | Authorized officer<br>WALTER P.<br>Telephone No. 1/53424/569 |

Form PCT/ISA/210 (second sheet) (July 1998)

# INTERNATIONAL SEARCH REPORT

Information [redacted] patent family members

Inter[redacted]nal application No.
PC[redacted]R 03/01549-0

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| JP A 20013439 22A2 | | none | |
| US A 20020063 671 | | none | |
| US A 20020084 965 | | none | |

522,007

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

19 JAN 2005

(43) International Publication Date
12 February 2004 (12.02.2004)

PCT

(10) International Publication Number
WO 2004/013682 A2

(51) International Patent Classification[7]: G02F

(21) International Application Number:
PCT/KR2003/001549

(22) International Filing Date: 31 July 2003 (31.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10-2002-0045815 2 August 2002 (02.08.2002) KR

(71) Applicant *(for all designated States except US)*: SAMSUNG ELECTRONICS CO., LTD. [KR/KR]; 416 Maetan-dong, Paldal-ku, Suwon-city, Kyungki-do 442-370 (KR).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: KIM, Jong-Seon [KR/KR]; Dongbu Apt. 102-301, Dokgok-dong, Pyeongtaek-city, Kyungki-do 459-801 (KR).

(74) Agent: YOU ME PATENT & LAW FIRM; Teheran Bldg., 825-33, Yoksam-dong, Kangnam-ku, Seoul 135-080 (KR).

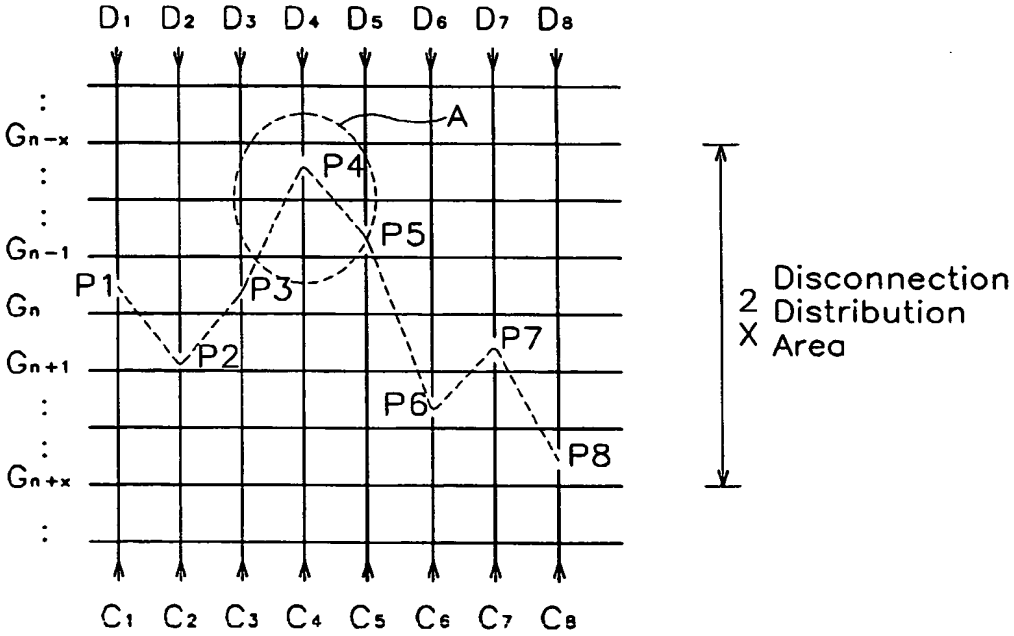
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *without international search report and to be republished upon receipt of that report*

*[Continued on next page]*

(54) Title: LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF




(57) Abstract: An LCD includes a plurality of upper, middle, and lower gate lines transmitting scanning signals provided on upper, middle, and lower areas, respectively, a plurality of pairs of upper and lower data lines transmitting data voltages, and a plurality of pixels connected to the gate lines and the data lines. The pixels are arranged in a matrix and include upper, middle, and lower pixels provided on the upper, the middle, and the lower areas, respectively. Each pair of upper and lower data lines are separated from each other at a disconnection, and the disconnections of the upper and the lower data lines are randomly distributed on the middle area.

WO 2004/013682 A2

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

## BACKGROUND OF THE INVENTION

**(a) Field of the Invention**

The present invention relates to a liquid crystal display and a driving method thereof.

**(b) Description of Related Art**

Recent trends of lightness and slimness of personal computers and television sets require lightness and slimness of display devices and thus flat panel displays such as a liquid crystal display (LCD) substitute cathode ray tubes (CRT).

An LCD includes two panels and a liquid crystal (LC) layer with dielectric anisotropy interposed between the two panels. The LCD displays desired images by adjusting electric field applied to the LC layer to control transmittance of light passing through the LC layer.

A typical LCD includes a plurality of the gate lines transmitting scanning signals, a plurality of data lines tra nsmitting data signals, and a plurality of pixels arranged in a matrix and including a plurality of switching elements such as TFTs connected to the gate lines and the data lines.

Scanning signals are sequentially applied to the gate lines to sequentially activate the switching elements connected to the gate lines and data voltages for the pixels connected to the activated switching elements are applied to the data lines. The data voltages are then applied to the pixels via the activated switching elements. All the gate lines are once scanned to make all the pixels be supplied with the data voltages in a frame.

Since the duration for one frame is fixed, for example, by one sixtieth seconds, higher resolution of LCDs, which requires more gate lines, reduces the scanning time for each gate line to yield insufficient application time of the data voltages and thus to deteriorate image quality.

A technique called "dual scan" is recently suggested for obtaining sufficient scanning time, which separately drives upper and lower halves of a display panel divided with respect to an imaginary straight line (referred to as a "disconnection line" hereinafter) parallel to the gate lines. An LCD suitable for the dual scan includes two sets of data lines and gate lines provided in the upper and the lower halves of the panel, respectively, and is provided with a pair of gate drivers and a pair of data drivers. The dual scan simultaneously scans the gate lines in the upper and the lower halves of the panels and thus increases the scanning time twice.

However, a conventional dual scan LCD has a problem that the difference in the luminance between the upper half and the lower half is easily recognized along the disconnection line although the magnitude of the luminance difference is small.

## SUMMARY OF THE INVENTION

A motivation of the present invention is to solve problems of a conventional art.

A liquid crystal display is provided, which includes: a plurality of first, second, and third gate lines transmitting scanning signals provided on first, second, and third areas, respectively; a plurality of pairs of first and second data lines transmitting data voltages, each pair of first and second data lines separated from each other at a disconnection; and a plurality of pixels connected to the gate lines and the data lines, arranged in a matrix, and including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively, wherein the disconnections of the first and the second data lines are randomly distributed on the second area.

Preferably, one of the first gate lines and one of the third gate lines are simultaneously scanned, and the second gate lines are scanned after the first and the third gate lines are scanned.

Each pair of first and second data lines are preferably supplied with a single data voltage during the scanning of each of the second gate lines.

It is preferable, the number of the first gate lines is equal to the number of the third gate lines, and the second area is disposed between the first area and the third area. The scanning directions for the first, the second, and the third gate lines may be the same.

The liquid crystal display may further include: first and second data drivers applying the data voltages to the first and the second data lines, respectively; a gate driver applying the scanning signals to the first, the second, and the third gate lines; and a memory storing image data corresponding to the data voltages and supplying the image data to the first and the second data drivers.

The image data are written in the memory in synchronization with a write clock and are read in synchronization with a read clock. The read clock preferably has a frequency substantially half of a frequency of the write clock.

Preferably, the image data for the first pixels and the third pixels are supplied to the first data driver and the second data driver, respectively, and the image data for the second pixels are supplied to both the first and the second data drivers.

A method of driving a liquid crystal display including a plurality of first, second, and third gate lines transmitting scanning signals provided on first, second, and third areas, respectively, a plurality of pairs of first and second data lines transmitting data voltages and separated from each other at a plurality of disconnections randomly distributed on the second area, and a plurality of pixels connected to the gate lines and the data lines and including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively, the method includes: sequentially applying scanning signals to the first gate lines and the third gate lines in pairs at the same time; applying data voltages for the first pixels and the third pixels to the first data lines and the second data lines, respectively; sequentially applying scanning signals to the second gate lines; and applying data voltages for the second pixels to both the first and the second data lines.

The application of scanning signals to the second gate lines is preferably performed after the application of scanning signals to the first gate lines and the third gate lines.

The method may further includes: writing image signals corresponding to the data voltages into a memory in synchronization with a write clock; reading out the image signals for the first and the third pixels in synchronization with a read clock preferably having a frequency substantially equal to half of a frequency of the write clock; converting the read-out image signals for the first and the third pixels into the data voltages; reading out the image signals for the second pixels in synchronization with the read clock; and converting the read-out image signals for the second pixels into the data voltages.

## BRIEF DESCRIPTION OF THE DRAWINGS

The above and other advantages of the present invention will become more apparent by describing preferred embodiments thereof in detail with reference to the accompanying drawings in which:

Fig. 1 is a block diagram of an LCD according to an embodiment of the present invention;

Fig. 2 illustrates an exemplary distribution of disconnections in an LCD according to an embodiment of the present invention;

Fig. 3 is a detailed diagram of a portion A shown in Fig. 2;

Fig. 4 is a timing diagram of an LCD according to an embodiment of the present invention; and

Fig. 5 is a schematic diagram of a memory according to an embodiment of the present invention.

## DETAILED DESCRITPION OF PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may,

however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

Now, liquid crystal displays and driving methods thereof according to embodiments of the present invention will be described in detail with reference to the accompanying drawings.

Fig. 1 is a block diagram of an LCD according to an embodiment of the present invention, Fig. 2 illustrates an exemplary distribution of disconnections in an LCD according to an embodiment of the present invention, and Fig. 3 is a detailed diagram of a portion A shown in Fig. 2.

Referring to Fig. 1, an LCD according to an embodiment of the present invention includes a LC panel 100, upper and lower data drivers 210 and 220, a gate driver 300, a memory unit 400, and a signal controller 500.

The LC panel 100 includes a plurality of the gate lines $G_1$-$G_m$ transmitting gate signals (also referred to as scanning signals), a plurality of upper and lower data lines $D_1$-$D_N$ and $C_1$-$C_N$ transmitting data voltages, and a plurality of pixels connected to the gate lines $G_1$-$G_m$ and the data lines $D_1$-$D_N$ and $C_1$-$C_N$.

Referring to Fig. 3, each pixel includes a LC capacitor $C_{LC}$ and a thin film transistor $T_i$ (i=1, 2, ...) connected thereto. The LC capacitor $C_{LC}$ includes a pixel electrode (not shown), a common electrode (not shown), and a LC layer (not shown) interposed therebetween, and a thin film transistor $T_i$ (i=1, 2, ...) has a gate connected to one of the gate lines $G_1$-$G_m$, a source connected to one of the data lines $D_1$-$D_N$ and $C_1$-$C_N$, and a drain connected to the pixel electrode of the LC capacitor $C_{LC}$.

The gate lines $G_1$-$G_m$ are grouped into an upper set including a plurality of gate lines $G_1$-$G_{n-x-1}$, a middle set including a plurality of gate lines $G_{n-x}$-$G_{n+x}$, and a lower set including a plurality of gate lines $G_{n+x+1}$-$G_m$ ($n \neq 2m$). The areas provided with the upper set, the middle set, and the lower set of gate lines $G_1$-$G_{n-x-1}$, $G_{n-x}$-$G_{n+x}$ and $G_{n+x+1}$-$G_m$ are referred to as an upper area 100A, a middle area 100B, and a lower area 100C, respectively.

According to another embodiment of the present invention, the gate lines are grouped into larger than three sets.

The upper data lines $D_1$-$D_N$ and the lower data lines $C_1$-$C_N$ are divided at disconnections Pi (i=1, 2, ...) that are randomly distributed on the middle area 100B, as shown in Fig. 2. In other words, the disconnections Pi according to an embodiment of the present invention, which separates the upper data lines $D_1$-$D_N$ and the lower data lines $C_1$-$C_N$, are irregularly distributed on the middle area 100B. For example, a line connecting the disconnections Pi (shown as a dotted line in the figures) is neither straight nor parallel to the gate lines $G_1$-$G_m$. Instead, the connecting line has a plurality of turning points. This irregular distribution of the disconnections Pi prevent easy detection of brightness difference near the disconnections Pi since human eyes easily recognize regular shapes such as straight lines and flat surfaces even though the brightness difference is very small.

The gate driver 300 is connected to the gate lines $G_1$-$G_m$ and applies a gate-on voltage to the gate lines $G_1$-$G_m$. According to an embodiment of the present invention, the gate driver 300 sequentially applies the gate-on voltage to the gate lines in pairs among the upper set and the lower set of gate lines $G_1$-$G_{n-x-1}$ and $G_{n+x+1}$-$G_m$, and thereafter, sequentially applies the gate-on voltage to the middle set of gate lines $G_{n-x}$-$G_{n+x}$. For example, the gate driver 300 sequentially applies the gate-on voltage to a first gate line $G_1$, to a second gate line $G_2$, ..., and a (n-x-1)-th gate line $G_1$-$G_{n-x-1}$ of the upper set of gate line $G_1$-$G_{n-x-1}$ in a downward direction, and, at the same time, the gate driver 300 sequentially applies the gate-on voltage to a first gate line $G_{n+x+1}$, to a second gate line $G_{n+x+2}$, ..., and a final gate line $G_m$ of the lower set of gate line $G_{n+x+1}$-$G_m$ in the downward direction. Thereafter, the gate driver 300 sequentially applies the gate-on voltage to a first gate line $G_{n-x}$, to a second gate line $G_{n-x+1}$, ..., and a final gate line $G_{n+x}$ of the middle set of gate line $G_{n-x}$-$G_{n+x}$ in the downward direction.

The upper and the lower data drivers 210 and 220 are disposed at the top and bottom of the LC panel 100, respectively, and apply data voltages to

the upper data lines $D_1$-$D_N$ and the lower data lines $C_1$-$C_N$, respectively, based on image signals from the memory unit 400.

The signal controller 500 receives image data DATA, a main clock MCLK, a horizontal synchronization signal Hsync, and a vertical synchronization signal Vsync from an external source, and generates necessary timing signals to be supplied to the memory unit 400, the gate driver 300, and the data drivers 210 and 220.

The memory unit 400 writes and reads image data DATA to be supplied to the upper data driver 210 and the lower data driver 220 in synchronization with a write clock WCLK and a read clock RCLK from the signal controller 500, respectively. The read clock RCLK has a frequency equal to half of the write clock WCLK. Although the memory unit 400 shown in Fig. 1 includes an upper memory and a lower the memory, it may have other configurations.

Now, an operation of an LCD according to an embodiment of the present invention is described in detail with reference to Figs. 4 and 5.

Fig. 4 is a timing chart of an LCD according to an embodiment of the present invention, and Fig. 5 is a schematic diagram of a memory unit.

The signal controller 500 receives image data DATA, a main clock MCLK, a vertical synchronization signal Vsync as a frame synchronization signal, and a horizontal synchronization signal Hsync.

The memory unit 400 writes the image data DATA in synchronization with the write clock WCLK from the signal controller 500. The image data DATA for the pixels in a first row, a second row, ..., a (n-x-1)-th row, a (n-x)-th row, ..., a (n+x-1)-th row, a (n+x)-the row, ..., and a last m-th row are sequentially written in the memory unit 400 in synchronization with a write clock WCLK. The image data DATA for the pixels on the second area 100B may be written into a portion of the upper memory or the lower memory.

The image data DATA stored in the memory unit 400 are read from the memory unit 400 in synchronization with a read clock RCLK and supplied to the upper data driver 210 or the lower data driver 210 and 220.

In detail, the signal controller 500 provides the read clock RCLK for the memory unit 400 such that the stored image data DATA for the pixels in pairs on the upper area 100A and the lower area 100C are read, which in turn are supplied to the upper data driver 210 and the lower data driver 220, respectively. After reading all the image data DATA for the pixels on the upper area 100A and the lower area 100C, the image data DATA for the pixels on the middle area 100B stored in the memory unit 400 are read out to be supplied to both the upper data driver 210 and the lower data driver 220.

The data drivers 210 and 220 receive the image data DATA, which are transmitted in synchronization with a clock HCLK, and convert the received image data DATA into analog data voltages. The upper data driver 210 and the lower data driver 220 apply the data voltages to the upper data lines $D_1$-$D_N$ and the lower data lines $C_1$-$C_N$, respectively, in response to a load signal LOAD from the signal controller 500.

In the meantime, the gate driver 300 applies a gate-on voltage (i.e., high voltage of scanning signals) to one of the upper set of gate lines $G_1$-$G_{n-x-1}$ and simultaneously to one of the lower set of gate lines $G_{n+x+1}$-$G_m$ in synchronization with a vertical synchronization start signal STV and a gate clock CPV from the signal controller 500. The application of the gate-on voltage to the gate lines $G_1$-$G_{n-x-1}$ and $G_{n+x+1}$-$G_m$ is performed in sequence from the first gate lines $G_1$ and $G_{n+x+1}$ to the last gate lines $G_{n-x-1}$ and $G_m$ in a downward direction. Thereafter, the gate driver 300 sequentially applies the gate-on voltage to the middle set of gate lines $G_{n-x}$-$G_{n+x}$ in the downward direction.

The application of the gate-on voltage turns on TFTs connected to the gate lines $G_1$-$G_m$ supplied with the gate-on voltage and the activated TFTs transmit the data voltages from the data drivers 210 and 220 to the pixel electrodes.

Although the data voltages for the pixels on the second area 100B are applied to both the upper data lines $D_1$-$D_N$ and the lower data lines $C_1$-$C_N$, only one of each pair of the upper and the lower data lines $D_1$-$D_N$ and $C_1$-$C_N$

can transmit a data voltage to a target pixel since each pixel is connected only one of the upper and the lower data lines $D_1$-$D_N$ and $C_1$-$C_N$.

According to another embodiment of the present invention, the first to the n-th gate lines $G_1$-$G_n$ are sequentially scanned and, at the same time, the (n+x+1)-th to the last gate lines $G_{n+x+1}$-$G_m$ are sequentially scanned. After the scanning of the gate line $G_n$, the (n+1)-th to the (n+x)-th gate lines $G_{n+1}$-$G_{n+x}$ are scanned in sequence.

For this purpose, an LCD according to another embodiment of the present invention includes an upper gate driver (not shown) connected to the first to the n-th gate lines $G_1$-$G_n$ and a lower gate driver (not shown) connected to the (n+1)-th to the m-th gate lines $G_{n+1}$-$G_m$, instead of a single gate driver, such that the upper gate driver and the lower gate driver scan the gate lines $G_1$-$G_n$ and $G_{n+1}$-$G_m$, respectively. For example, the upper gate driver sequentially scans from the first gate line $G_1$ to the n-th gate line $G_n$, while the lower gate driver sequentially scans from the (n+x+1)-th gate line $G_{n+x+1}$ to the last gate line $G_m$ and then scans from the (n+1)-th gate line $G_{n+1}$ to the (n+x)-th gate line $G_{n+x+1}$ after the scanning of the (n-x)-th to the n-th gate lines $G_{n-x}$-$G_n$ is finished.

The scanning scheme such as the scanning direction is not limited to those described above, but it can be varied and modified.

As described above, the embodiments of the present invention randomly distribute the disconnections between the upper data lines and the lower data lines such that a line connecting the disconnections does not exhibit regularity, thereby preventing the brightness difference near the disconnections from being clearly recognized.

Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

**WHAT IS CLAIMED IS:**

1. A liquid crystal display, comprising:

a plurality of first, second, and third gate lines transmitting scanning signals provided on first, second, and third areas, respectively;

a plurality of pairs of first and second data lines transmitting data voltages, each pair of first and second data lines separated from each other at a disconnection; and

a plurality of pixels connected to the gate lines and the data lines, arranged in a matrix, and including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively,

wherein the disconnections of the first and the second data lines are randomly distributed on the second area.

2. The liquid crystal display of claim 1, wherein one of the first gate lines and one of the third gate lines are simultaneously scanned, and the second gate lines are scanned after the first and the third gate lines are scanned.

3. The liquid crystal display of claim 1, wherein each pair of first and second data lines are supplied with a single data voltage during the scanning of each of the second gate lines.

4. The liquid crystal display of claim 1, wherein the number of the first gate lines is equal to the number of the third gate lines, and the second area is disposed between the first area and the third area.

5. The liquid crystal display of claim 4, wherein the scanning directions for the first, the second, and the third gate lines are the same.

6. The liquid crystal display of claim 1, further comprising:

first and second data drivers applying the data voltages to the first and the second data lines, respectively;

a gate driver applying the scanning signals to the first, the second, and the third gate lines; and

a memory storing image data corresponding to the data voltages and supplying the image data to the first and the second data drivers.

7. The liquid crystal display of claim 6, wherein the image data are written in the memory in synchronization with a write clock and are read in synchronization with a read clock having a frequency substantially half of a frequency of the write clock.

8. The liquid crystal display of claim 6, wherein the image data for the first pixels and the third pixels are supplied to the first data driver and the second data driver, respectively, and the image data for the second pixels are supplied to both the first and the second data drivers.

9. The liquid crystal display of claim 8, wherein one of the first gate lines and one of the third gate lines are simultaneously scanned, and the second gate lines are scanned after the first and the third gate lines are scanned.

10. The liquid crystal display of claim 6, wherein the number of the first gate lines is equal to the number of the third gate lines, and the second area is disposed between the first area and the third area.

11. The liquid crystal display of claim 10, wherein the scanning directions for the first, the second, and the third gate lines are the same.

12. A method of driving a liquid crystal display including a plurality of first, second, and third gate lines transmitting scanning signals provided on first, second, and third areas, respectively, a plurality of pairs of first and second data lines transmitting data voltages and separated from each other at a plurality of disconnections randomly distributed on the second area, and a plurality of pixels connected to the gate lines and the data lines and including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively, the method comprising:

sequentially applying scanning signals to the first gate lines and the third gate lines in pairs at the same time;

applying data voltages for the first pixels and the third pixels to the first data lines and the second data lines, respectively;

sequentially applying scanning signals to the second gate lines; and

applying data voltages for the second pixels to both the first and the second data lines.

13. The method of claim 12, wherein the application of scanning signals to the second gate lines is performed after the application of scanning signals to the first gate lines and the third gate lines.

14. The method of claim 12, further comprising:

writing image signals corresponding to the data voltages into a memory in synchronization with a write clock;

reading out the image signals for the first and the third pixels in synchronization with a read clock;

converting the read-out image signals for the first and the third pixels into the data voltages;

reading out the image signals for the second pixels in synchronization with the read clock; and

converting the read-out image signals for the second pixels into the data voltages.

15. The method of claim 14, wherein the read clock has a frequency substantially equal to half of a frequency of the write clock.

FIG.1

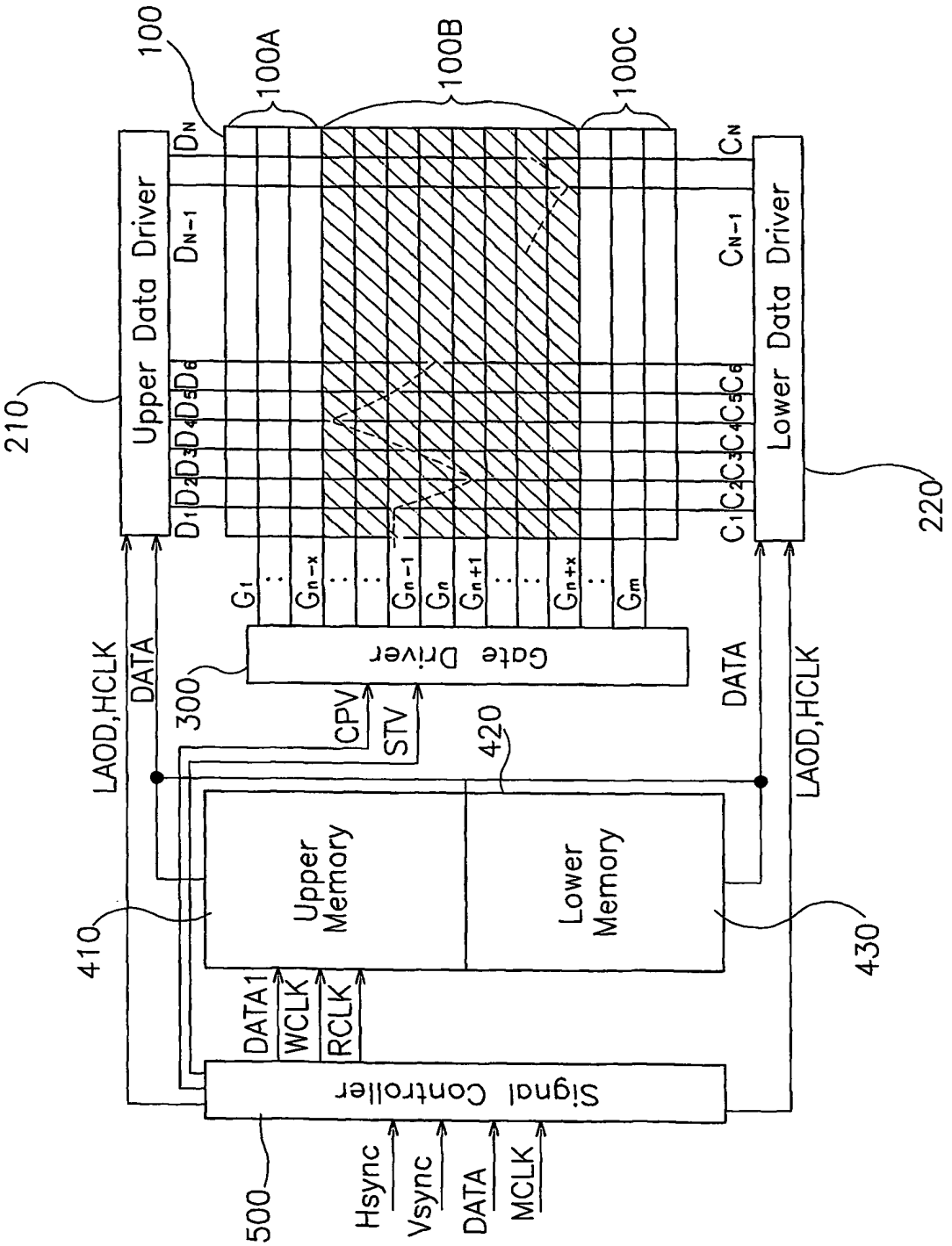

100
100A
100B
100C
Upper Data Driver
Lower Data Driver
210
220
Gate Driver
300
Upper Memory
Lower Memory
410
420
430
Signal Controller
500
LAOD,HCLK
DATA
CPV
STV
DATA1
WCLK
RCLK
Hsync
Vsync
DATA
MCLK

FIG.2

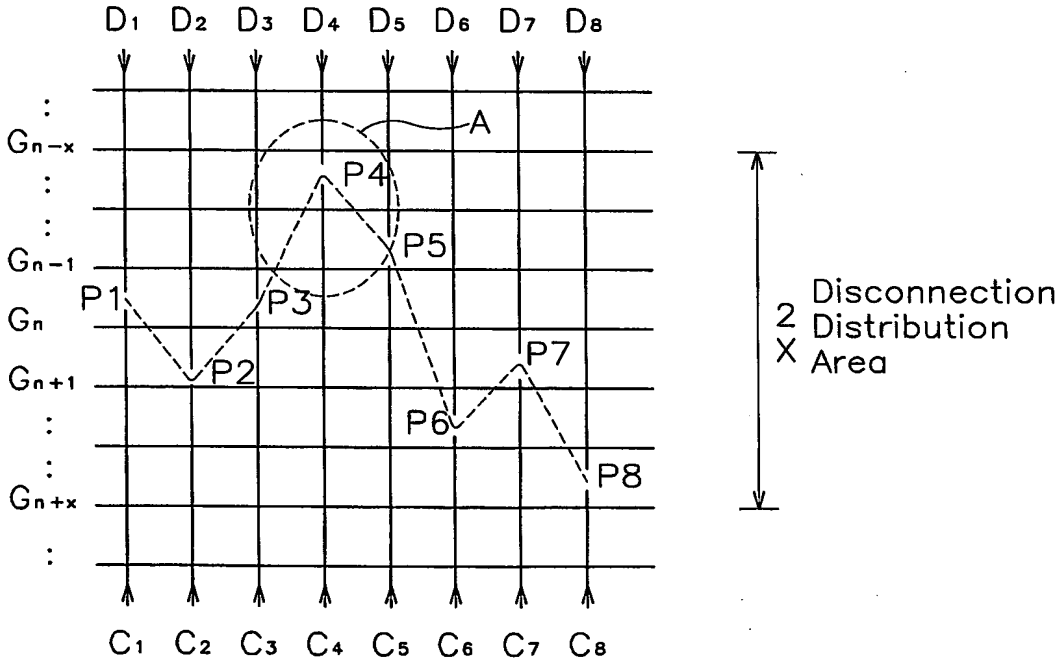

D1 D2 D3 D4 D5 D6 D7 D8
Gn-x
Gn-1
Gn
Gn+1
Gn+x
A
P1
P2
P3
P4
P5
P6
P7
P8
C1 C2 C3 C4 C5 C6 C7 C8
2X
Disconnection Distribution Area

FIG.3

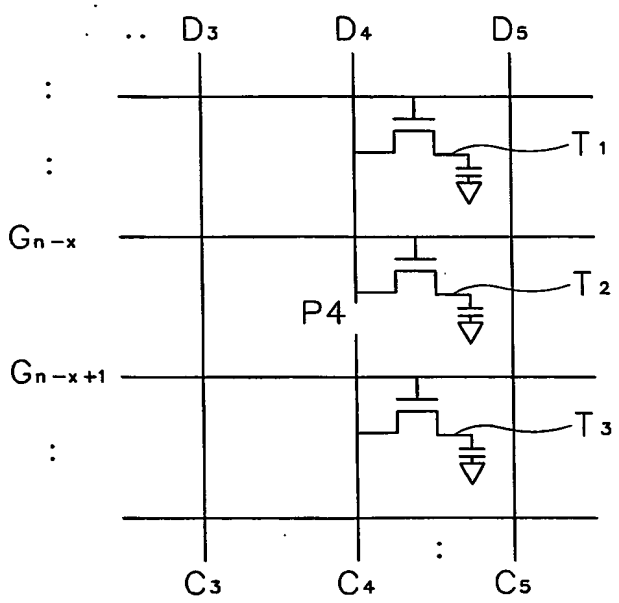
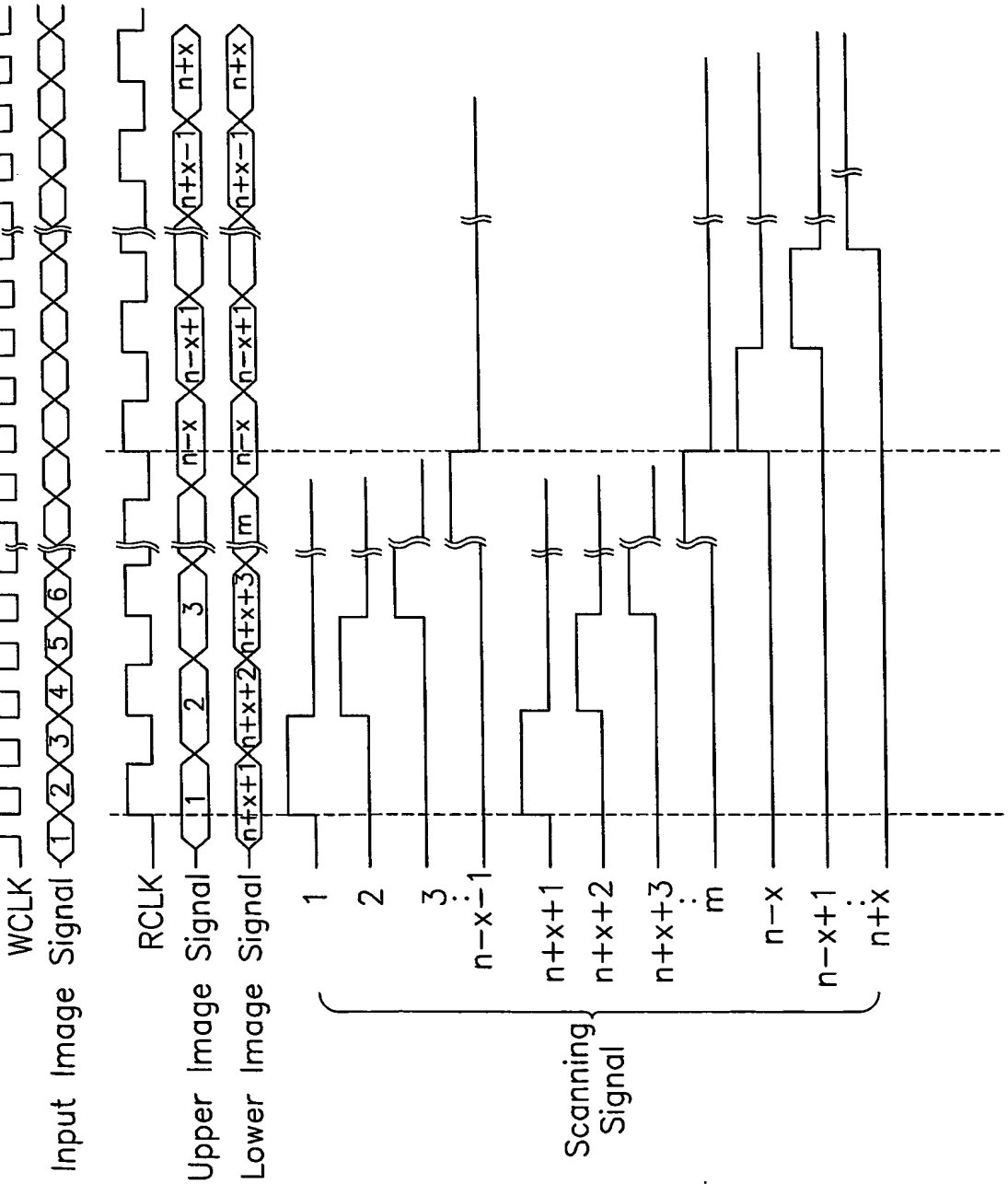
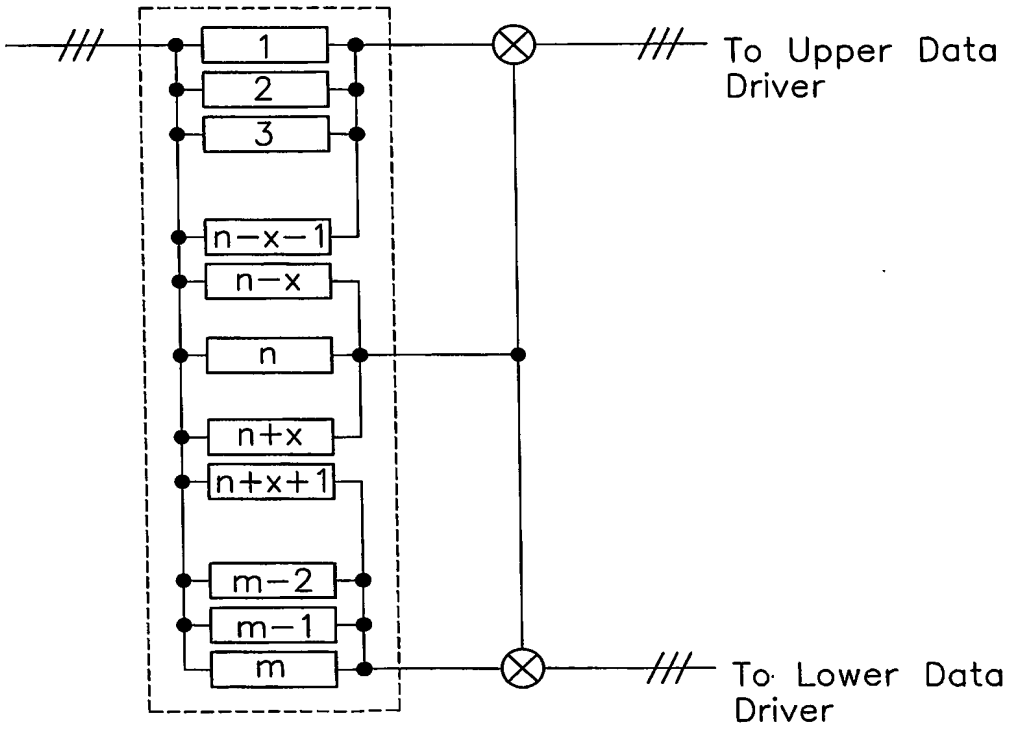


FIG.4


WCLK
Input Image Signal
1
2
3
4
5
6
RCLK
Upper Image Signal
Lower Image Signal
n+x+1
1
n+x+2
2
n+x+3
3
m
n-x
n-x+1
n+x
Scanning Signal
1
2
3
n-x-1
n+x+1
n+x+2
n+x+3
m
n-x
n-x+1
n+x

5/5

FIG.5


1
2
3
n−x−1
n−x
n
n+x
n+x+1
m−2
m−1
m
To Upper Data Driver
To Lower Data Driver